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# Integrated Very High Frequency Switch Mode Power Supplies: Design Considerations

Jens Christian Hertel, *Student Member, IEEE*, Yasser Nour, *Member, IEEE*, and Arnold Knott

**Abstract**—This paper presents a power supply using an increased switching frequency to minimize the size of energy storing components, thereby addressing the demands for increased power densities in power supplies. 100 MHz and higher switching frequencies have been used in resonant power converters, which along with the possible integration of passive components on silicon wafer, present a beneficial solution in applications such as mobile phones. This paper presents a design for a 9 W class E resonant power converter in an 0.18  $\mu\text{m}$  CMOS process. The converter is driven by a self oscillating gate drive, which is presented in an in-depth mathematical analysis. The gate resistance of the designed transistors is of critical importance in order to achieve the correct phase shift required for zero-voltage-switching. The Z-parameter method is used to characterize the transistors which is verified through simulations. The required spiral inductors was modeled, and simulations show Q values of as high as 14 at a switching frequency of 250 MHz. Simulations of the converter show an efficiency of 55 % with a self oscillating gate drive. However the modeled inductor was not adequate for operating with the self oscillating gate drive, presenting a future challenge for power supplies on chip.

**Index Terms**—DC-DC power converters, Radiofrequency integrated circuits, VHF circuits, Integrated circuit modeling, Zero voltage switching

## I. INTRODUCTION

Consumer, industrial and automotive electronics are ever decreasing in size and consequently, the demand for smaller power supplies is increasing. The size of power supplies can be reduced through increasing the switching frequency, minimizing the energy storing components. In the classic hard-switched DC/DC Switch Mode Power Supply (SMPS) energy is lost every time the power transistor is turned on and off. The switching loss thus increases with switching frequency. This problem has led to the combination of power electronics and radio frequency technology, known as resonant power converters. The advantages are the elimination of switching losses, using Zero Voltage Switching (ZVS) and in some cases also Zero Current Switching (ZCS). The technology has proved itself, with switching frequencies in the Very High Frequency (VHF) band [1]–[4]. So far this has mainly been

applied to LED drivers [5]–[7], but has far more possible applications. The energy storing components are small enough that integration onto a silicon wafer is possible. Achieving a fully integrated SMPS would be useful in e.g. cellphone applications, where size and high production volume are important parameters.

In [8] two types of integrated power supplies are defined, Power Supply in Package (PwrSiP) and Power Supply on Chip (PwrSoC). PwrSiP integrates the power transistors and control circuitry monolithically, with the energy storage integrated into the package, e.g. [9]. There are various products available on the market, from several companies, [10]–[14] that implement power supplies in complete packaging. PwrSoC has all the components integrated into the same die. The advantage of the fully monolithic converter is reduced parasitic capacitance and inductance generated from connections needed in the PwrSiP solution. This is important when increasing the switching frequency above 100 MHz [1]. On the other hand the quality of most inductors on chips today are very low. A possible solution would be excluding the inductors using a switched capacitor network [15], [16], however these are often not efficient outside their optimum voltage conversion ratio [17]. Achieving an efficient PwrSoC solution would require an inductor having a high quality factor [8], [18]. The PwrSiP products available have power densities of 0.2-0.5 W/mm<sup>3</sup>, and efficiencies around 90-95 % [8]. PwrSoC is still a very new concept, and research have achieved power densities comparable to the PwrSiP products with efficiencies ranging from 30-80 % [8]. Dibene et.al. [19] presents a 400 A PwrSoC with a power density of 8 W/mm<sup>3</sup>, and an efficiency just below 80 %, using multiple phases, and advanced control mechanisms.

A possible application within the field of cellphones is a power supply for an audio amplifier. There are many ways to amplify audio from an inherently inefficient class AB amplifier to the ideally lossless class D amplifier [20]. The quiescent current in the class AB topology generates constant losses, making it undesirable for a cellphone application. The more commonly used class D amplifier is, due to the Pulsed-Width Modulation (PWM) technique, ideally lossless. However a side effect of the PWM is increased EMI [21]. If a power supply is designed to only deliver the required power of a class AB amplifier, eliminating the quiescent current, then efficiencies can be increased from the maximum of 78.5 % to ideally 100 %. This is effectively known as a class H amplifier.

This paper presents an integrated class E resonant power converter supplying a class AB audio amplifier. It is supplying a maximum output voltage of 6 V from a Li-Ion battery, assumed to have constant 3.7 V input. The output power is

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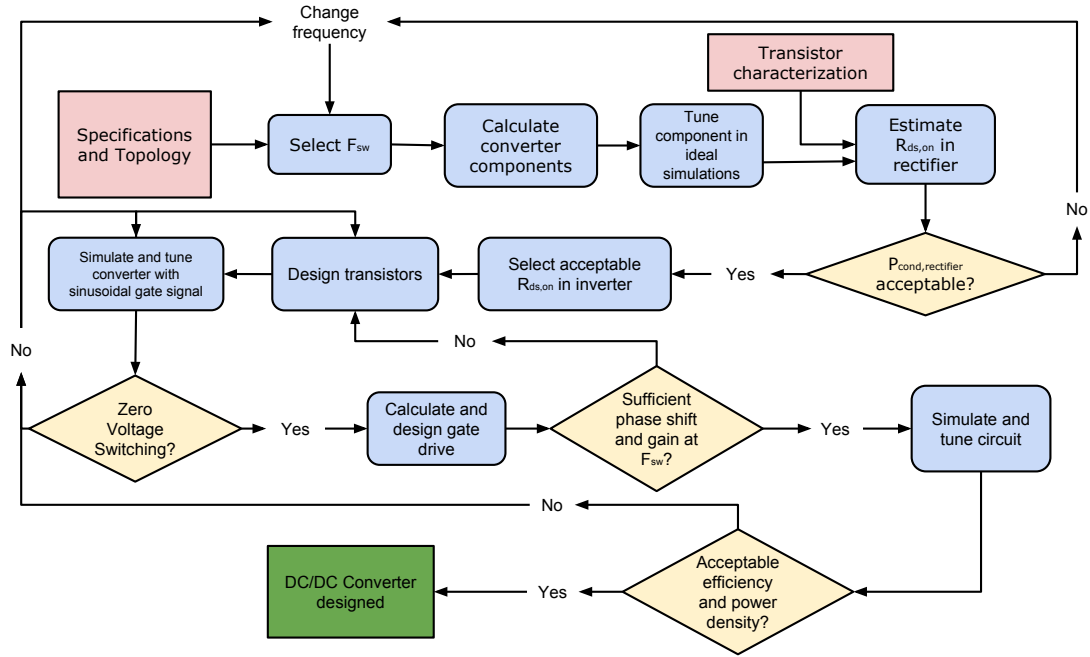


Fig. 1. Flowchart describing the design procedure of an integrated VHF resonant power supply

TABLE I  
SPECIFICATIONS FOR THE POWER SUPPLY

$V_{in}$	3.7 V
$V_{out}$	6 V
$P_{out}$	9 W
Process	20 V 0.18 $\mu\text{m}$ CMOS

9 W in a 4  $\Omega$  speaker. The power supply is designed in a 20 V 0.18  $\mu\text{m}$  CMOS process, with a listed breakdown voltage of 27 V. The specs can be seen in table I. It is noted that for this to be used in a class H amplifier, it should track an audio sample, and supply the output accordingly. The design of the tracking circuitry has not been carried out.

Section II presents the design flow for the resonant power converter. The converter topology will be discussed and presented in section II-A. The power losses are introduced in section II-B. The device parasitics are discussed and a method for extracting them is presented in section II-C. Section II-D presents the self-oscillating gate drive, along with the mathematical equations underpinning its operation. Section II-E discusses inductors on a chip which is followed by section III, where the final design is presented, and the results of the simulations are shown. Finally, section IV concludes on the achieved results.

## II. DESIGN PROCEDURE

The design procedure is presented in fig. 1. All the relevant theories will be presented in-depth in the following. This procedure was developed for designing a Class E resonant converter. Similar theories applies to other resonant power converters, and the procedure can be modified to fit the relevant equations. The main design variable in this procedure is the frequency. When a switching frequency has

been selected the component values are calculated and tuned in ideal simulations. The higher the frequency, the smaller the converter. However in most resonant power converters the output capacitance of a transistor is used as a design parameter [1], [5]. This capacitance is proportional to the size of the transistor, which again is inversely proportional to the drain source resistance of the transistor. At higher frequencies the requirements for smaller capacitances results in higher conduction losses. This will set the first limitation. Following this, the losses in the inverter are calculated, and the transistor in the inverter is designed accordingly. Some tuning of the resonant components might be necessary after introducing the models of the power transistors. When this has been done, the self-oscillating gate drive can be designed. If the gate drive can not achieve a desired phase shift and gain, the designer must redesign the transistors. Final simulations must be carried out, to confirm a working and acceptable power converter. If one is unable to obtain ZVS or an acceptable efficiency and power density, the designer must either redesign the transistors, or ultimately limit the switching frequency of the converter.

### A. Converter Topology

The topology selection is limited to the resonant power converters. Among these, three topologies are often used in the VHF range; the class DE [22]–[24], SEPIC [25]–[27], and class E converter [28], [29], shown in fig. 2. They all work in a similar way with an inverter and a rectifier part. For the class DE and class E the inverter and rectifier can be interchanged. While the class DE converter (fig. 2a) only contains one resonant inductor, preferable in an integrated circuit, it also has three high side semiconductors. High side semiconductors, on a silicon wafer, requires their own wells, which is difficult to implement, and involves more advanced

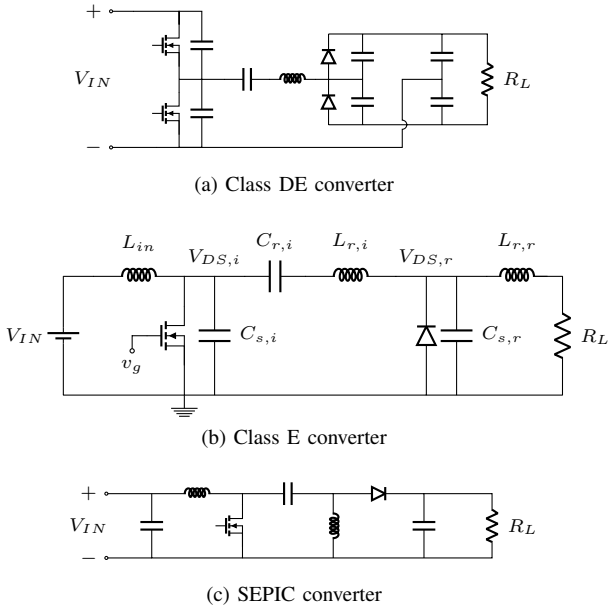


Fig. 2. Resonant Power Converters

processes, such as triple well or Silicon on Insulator (SOI). Furthermore, it adds parasitic capacitances through body and substrate, which will complicate higher frequency design.

The SEPIC converter (fig. 2c) also has a high side diode. It does have one less inductor compared to the class E, and the trade off between one less inductor and a high side diode could be investigated further. However, diodes capable of working in frequencies above 100 MHz are not commonly available in CMOS design kits. At very high frequencies, the conductivity modulation of power diodes has a tremendous contribution in the total loss. This effect was described in [30], [31]. Schottky diodes are the most suitable devices for very high frequency converters due to their low forward voltage drop and high switching speeds. Even with discrete schottky diodes, which outperform the integrated devices, forward recovery voltage is very severe. For a few nanoseconds the forward voltage increases by 50 %, generating unacceptable losses [32]. In high output voltage, low output current applications, diodes might be favorable.

Consequently the class E converter (fig. 2b) is deemed the most feasible to investigate for an integrating purpose, even though it has three inductors in total. The rectifier is usually implemented with a diode, but it can be exchanged for a synchronous transistor, avoiding the requirements of a diode capable of handling the high frequency. The shunt capacitances  $C_{s,i}$  and  $C_{s,r}$  of the inverter and the rectifier respectively at higher frequencies are so small that they are realized using the parasitic capacitances of the MOSFETs. In the inverter the

input inductor is designed to match the shunt capacitance of the transistor. In the rectifier the transistor is designed such that the output capacitance matches the selected switching frequency.

1) *Class E Inverter*: The class E inverter has two conditions in relation to the load,  $R_i$ , and the shunt capacitance,  $C_{s,i}$ , that must be met, to achieve both ZVS and ZCS. From [33] they are given in (1) and (2) at the bottom of this page.  $D_{inv}$  is the duty cycle of the inverter,  $f_s$  is the switching frequency and  $\phi_i$ , the phase of the current, is given by:

$$\phi_i = \pi + \arctan \left( \frac{\cos(2\pi D_{inv}) - 1}{2\pi(1 - D_{inv}) + \sin(2\pi D_{inv})} \right) \quad (3)$$

In the VHF inverter the shunt capacitance needed to achieve both ZVS and ZCS often is much lower than any achievable output capacitance of the MOSFET. The size of the transistor determines the output capacitance, and the drain-to-source resistance  $R_{ds,on}$ . Designing for a very low output capacitance requires a small transistor resulting in a higher  $R_{ds,on}$ . As a result the requirements for the frequency are hard to meet. Adjusting the input inductance can however compensate for this requirement, to ensure that ZVS is still achieved. This is well described in [34]. The load,  $R_i$ , on the inverter is simpler to achieve, either by designing the rectifier accordingly, or adding a matching circuit [35]. The latter is not explored in this paper.

The components are calculated from [36]. Assuming that the voltage across the drain-source of the transistor is half a sine wave when it is on, and zero otherwise, the RMS voltage of transistor drain-to-source can be calculated from (4). The output RMS voltage is calculated from the required load and output power (5). The required reactance of the reactance circuit can then be calculated from (6).

$$V_{DS,i,rms} = V_{IN} \frac{\pi}{2(1 - D_{inv})} \sqrt{\frac{(1 - D_{inv})}{2}} \quad (4)$$

$$V_{DS,r,rms} = \sqrt{P_{OUT} R_i} \quad (5)$$

$$\begin{aligned} X_{RC} &= R_i \sqrt{\left( \frac{V_{DS,i,rms}}{V_{DS,r,rms}} \right)^2 - 1} \\ &= \omega_r L_{r,i} - \frac{1}{\omega_r C_{r,i}} \end{aligned} \quad (6)$$

The RMS voltage of the output cannot exceed the RMS voltage of the drain-source voltage of the transistor. This gives rises to some limits on the duty cycle when the class E inverter is working in a step-up configuration. The needed inductance

$$R_i = \frac{2 \sin^2(\pi D_{inv}) \sin^2(\pi D_{inv} + \phi_i)}{\pi^2 (1 - D_{inv})^2} \cdot \frac{V_{IN}^2}{P_{out}} \quad (1)$$

$$f_{s,max} = \left( \frac{(1 - D_{inv})^2 \pi}{\tan(\pi D_{inv}) \tan(\pi D_{inv} + \phi_i) \tan(\pi D_{inv} + \phi_i)} \right) \cdot \frac{P_{out}}{2\pi C_{s,i} V_{IN}^2} \quad (2)$$

and capacitance in the resonant tank is found using the right hand side of (6),  $\omega_r$  is resonance frequency of the LC tank:

$$\omega_r = \frac{2\pi f_s}{2(1 - D_{inv})} \quad (7)$$

To ensure ZVS  $L_{in}$  is designed to match reactance of the output capacitance of the transistor and resonance tank [34]. The output capacitance is scaled to its effective capacitance,  $C_{s,eff} = C_{s,i}/(1 - D_{inv})$ . [5].

$$\frac{1}{\omega_r C_{s,eff}} = \frac{1}{\omega_r L_{in} + \frac{1}{X_{RC}}} \Leftrightarrow L_{in} = \frac{1}{\omega_r \left( \omega_r C_{s,eff} - \frac{1}{X_{RC}} \right)} \quad (8)$$

The output capacitance is assumed linear, ignoring its voltage dependencies.

2) *Class E Rectifier*: In the class E rectifier the passive components are designed in such a way that the rectifier is seen as a resistive load at the switching frequency [35]. The current into the rectifier is assumed to be sinusoidal. From [33] the shunt capacitance and resonance inductance, is given in (9) at the bottom of this page. The loading of the inverter is important to achieve ZVS. The components calculated ensure that the input resistance to the rectifier,  $R_i$ , is resistive at the desired switching frequency. The required input impedance of the rectifier is achieved by adjusting the duty cycle [2]. See (10) at the bottom of the current page.

3) *Components*: With the above described equations a set of components can be calculated, and through simulation tune them, to achieve ZVS. To achieve the correct loading the duty cycles of the inverter and rectifier is selected as close to 50 %, which is a requirement for the used gate drive. From (1) and (10) the two duty cycles are connected, to achieve optimum performance. If a duty cycle in the inverter of 60 % is chosen, then the calculated duty cycle in the rectifier is 43 %. The calculated and simulated components is listed in table II. The simulated components had to be tuned. The output power of the calculated inverter was lower than expected, due to not having pure sinusoidal current in the tank, and to increase it the resonance inductance  $L_{r,i}$  was increased. To match the effect of the increased inductance, the input choke  $L_{in}$ , was adjusted, to ensure ZVS.

### B. Power Loss Estimation in MOSFET

The resonant power conversion eliminates the switching losses known from hard switching applications. From [37] the power losses associated with a MOSFET in a resonant power converter can be separated into three parts - the conduction

TABLE II  
CALCULATED AND SIMULATED COMPONENT-VALUES OF A 250 MHZ CLASS E CONVERTER

Inverter		
Component	Calculated	Simulated
$L_{in}$	455 pH	750 pH
$C_{s,i}$	300 pF	300 pF
$C_{r,i}$	300 pF	300 pF
$L_{r,i}$	2.3 nH	3.5 nH
Rectifier		
Component	Calculated	Simulated
$R_i$	1.43 $\Omega$	-
$C_{s,r}$	120 pF	140 pF
$L_{r,r}$	4.49 nH	4.5 nH
$C_{out}$	80 nF	80 nF

loss, the off-state conduction loss due to the ESR in the shunt capacitance of the MOSFET, and the gate losses determined by the gate resistance and input capacitance.

$$P_{cond} = R_{ds,on} I_{sw,rms}^2 \quad (11)$$

$$P_{off,cond} = \left( \frac{I_{off,rms}}{C_{OSS} + C_{ext}} \right)^2 R_{OSS} C_{OSS}^2 \quad (12)$$

$$P_{gate} = 2 (\pi V_{gate,AC-pk} f_{sw})^2 R_g C_{ISS}^2 \quad (13)$$

$R_{OSS}$  is the series resistance associated with the shunt capacitance. The capacitances  $C_{ISS}$  and  $C_{OSS}$  are the collective capacitance seen on gate and drain respectively.

$$C_{OSS} = C_{gd} + C_{ds}$$

$$C_{ISS} = C_{gd} + C_{gs}$$

The total loss from the transistor is:

$$P_{tot,sw} = P_{cond} + P_{off,cond} + P_{gate} \quad (14)$$

### C. Characterization of Transistor

When designing a class E converter with discrete components the choice of transistors are limited to commercially available discrete parts. Often the transistor is described with the needed parameters available from the data sheet. In the integrated circuit the parameters required to design a DC-DC converter are not readily available. Many of the available process technologies have different purposes, and extracting the parameters directly from the documentation are tedious and time consuming. Therefore, another method is necessary.

The voltage stresses on the switches in a class E converter are often four times the input or output voltages [33]. To

$$C_r = \frac{1}{2\pi \omega_r R_L} \cdot \left( 1 - 2\pi^2(1 - D_{rec})^2 - \cos(2\pi D_{rec}) + \frac{[2\pi(1 - D_{rec}) + \sin(2\pi D_{rec})]^2}{1 - \cos(2\pi D_{rec})} \right) \quad \wedge \quad L_r = \frac{1}{\omega_r^2 C_r} \quad (9)$$

$$\frac{R_i}{R_L} = 2 \sin^2(\phi_r) \Leftrightarrow \sqrt{\frac{R_i}{2 R_L}} = \arctan \left( \frac{1 - \cos(2\pi D_{rec})}{2\pi(1 - D_{rec}) + \sin(2\pi D_{rec})} \right) \quad (10)$$

support this a technology with medium to high voltage capabilities was necessary. In this design a 0.18  $\mu\text{m}$  20 V process was used, with a breakdown voltage of 27 V. The simulation models available are level 49 HSPICE models, which are an enhanced BSIM3V3 model, especially for use with HSPICE.

The six most important parasitics of the transistor are the gate- ( $R_g$ ) and drain-source ( $R_{ds,on}$ ) resistance and the gate-source-, gate-drain- and drain-source capacitances ( $C_{gs}$ ,  $C_{gd}$  and  $C_{ds}$  respectively). Lastly the series resistance associated with the drain-source capacitance,  $R_{OSS}$ , is important to determine the off state losses. Fig. 3 illustrates the most important parasitics.

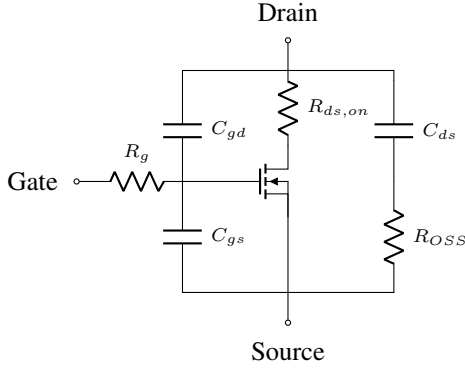


Fig. 3. Transistor with Parasitic Components

To extract the parasitics of the transistor, the two-port Z-parameter analysis is used. It is noted that the Z-parameter method creates a small signal equivalent model; however, by sweeping the frequencies and voltages, the large signal behavior can be derived [37], [38].

The described method of analyzing a circuit is done with a network-analyzer. It is often used in characterization of RF MOSFETs e.g [39]–[43] at frequencies above 10 GHz. These models are much more detailed than those of regular power MOSFETs. In the following, the simplest possible setup and analysis is described and the method is verified with a known device.

The two ports are connected to gate-source and drain-source respectively. Two equations govern the voltages, here shown on matrix-form:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \Leftrightarrow \vec{V} = \vec{Z} \cdot \vec{I} \quad (15)$$

Now applying current vectors, the expression for each Z-parameter in the matrix can be derived. To find the capacitances, the resistive parts of the circuit is ignored - see (16). Similarly the other parameters are derived, and the desired impedances are isolated in (17), (18) and (19).

$$Z_{C_{gs}} = \Im \left\{ -\frac{z_{11}z_{22} - z_{12}z_{21}}{z_{21} - z_{22}} \right\} \quad (17)$$

$$Z_{C_{gd}} = \Im \left\{ \frac{z_{11}z_{22} - z_{12}z_{21}}{z_{21}} \right\} \quad (18)$$

$$Z_{C_{ds}} = \Im \left\{ \frac{z_{11}z_{22} - z_{12}z_{21}}{z_{11} - z_{21}} \right\} \quad (19)$$

Note that in the above equations the parameters  $z_{mn}$  are only the imaginary part of the Z-parameters, giving the capacitances. For the resistive elements  $R_g$  and  $R_{OSS}$ , the S-parameter measures are more complicated. The gate resistance can be estimated from the parameter  $z_{11}$ . The  $z_{22}$  parameter are at  $V_{gs} \geq V_{th}$  equal to the drain source on resistance of the device. At  $V_{gs} \leq V_{th}$ , and ignoring the resistive influence on the capacitances,  $R_{OSS}$  can be estimated using (21).

$$\Re\{z_{11}\} = R_g \quad (20)$$

$$\Re\{z_{22}\} = \begin{cases} \frac{1}{R_{OSS} \cdot C_{gd}^2 \cdot \omega^2} & , \text{ for } V_{gs} = 0 \\ R_{ds,on} & , \text{ for } V_{gs} > V_{th} \end{cases} \quad (21)$$

Another method to extract  $R_{ds,on}$  is to use a DC current-source connected at the drain, sweeping the gate voltage, and sampling the drain voltage. This gives some limitations to how the models work, because they are forced in saturation. To avoid this, instead a small voltage on the drain will keep the transistor in its linear region, where it is used, and sweeping the gate-voltage, the current is read. This method is used for extracting the parameters of the designed device.

1) *Verification of Characterization:* To verify that this way of measuring the parasitics is correct, a IRF5802 from International Rectifier with a highly detailed datasheet and SPICE model was used. The datasheet for IRF5802 contains graphs of  $R_{ds,on}$  vs. gate-source voltage ( $V_{gs}$ ), and capacitances  $C_{iss}$ ,  $C_{oss}$  and  $C_{rss}$  vs. drain-source voltage ( $V_{ds}$ ). Its SPICE model is a sub circuit, modeled to the behavior of the device at 1 MHz.

In the datasheet the capacitances are measured at 1 MHz and a gate-source voltage of 0 V, and the simulation and measurements are carried out with the same conditions. Fig. 4 shows the results of the simulations and datasheet values. The capacitances fit their datasheet values. For the  $R_{ds,on}$  values the Z-parameter analysis does not accurately produce the same results as the datasheet in values of  $V_{gs} < 10$  V; on the other hand, the method described in the datasheet, with a DC current source, produce close to the expected results.

Furthermore, measurements of the IRF5802 was carried out, to confirm the simulations. It was done using a Agilent 4396B network analyzer together with a HP 85046A S-parameter Test set. The measurement circuit can be seen in fig. 5a and the resulting measured capacitances can be seen in fig. 5b. The measured data matches the datasheet values.

$$v_1 \Big|_{i_2=0} = \Im\{z_{11}\} \cdot i_1 = Z_{C_{gs}} \cdot i_{C_{gs}} = Z_{C_{gs}} \cdot \frac{Z_{C_{gd}} + Z_{C_{ds}}}{Z_{C_{gd}} + Z_{C_{ds}} + Z_{C_{gs}}} \cdot i_1 \Rightarrow \Im\{z_{11}\} = Z_{C_{gs}} \cdot \frac{Z_{C_{gd}} + Z_{C_{ds}}}{Z_{C_{gd}} + Z_{C_{ds}} + Z_{C_{gs}}} \quad (16)$$

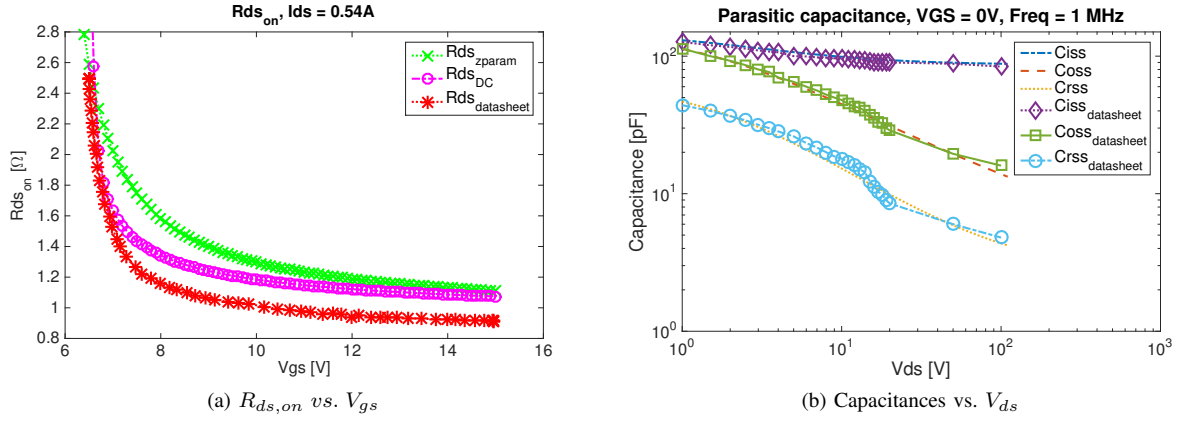
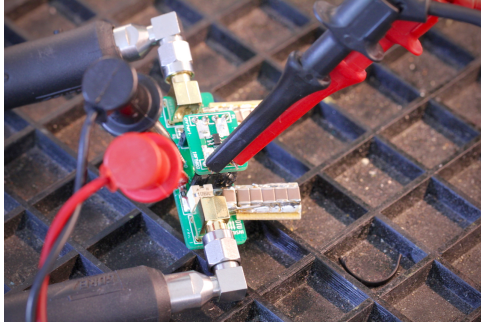


Fig. 4. Simulated results of the Z-parameter analysis



(a) Picture of measurement circuit

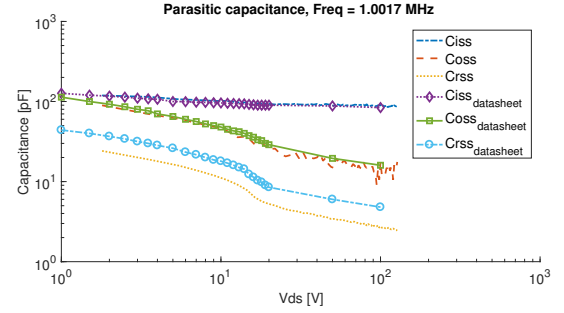
(b) Measured Capacitances using the proposed Z-parameter analysis. ( $V_{gs} = 0$ )

Fig. 5. Measurement of IRF5802

2) *Transistor Estimation:* To ease the process of estimating the parameters of the transistor, a unit-transistor with an  $R_{ds,on}$  of  $1\ \Omega$  is designed. Parallel coupling two  $1\text{-}\Omega$ -unit ( $2 \times 1\text{-}\Omega$ -unit) transistors halves the  $R_{ds,on}$  and doubles the capacitance. The simulated results is shown in fig. 6 and 7.

Fig. 6 shows the resistances. Both methods of extracting the  $R_{ds,on}$  produce similar results. At 5 V gate-to-source voltage the expected on-resistance is approximately  $1\ \Omega$ .

Fig. 7 provides the capacitances - both versus voltage and frequency. The gate-drain and gate-source capacitance are linear over the voltage. While this is the results of the model, experimental data might reveal some non-linearities. However, as these devices are vertical CMOS devices, their gate-related capacitances are often more linear, than what is known from open lateral power MOSFET. The drain to source capacitance vary largely over both frequency and voltage.

The results of  $z_{22}$  parameter at  $V_{gs} = 0$ , reveal a large resistance associated with the drain-source capacitance of  $3.75\ \Omega$ . This resistance will result in off state losses. The resulting parasitic elements of the unit transistor are summarized in table III.

#### D. Driving the Transistor

Driving a transistor at high frequency is a challenge. In VHF converters it is very impractical to drive the gate with a PWM signal. There are several methods to drive the gate, either with an externally generated signal, or with a self-oscillating circuit.

TABLE III  
PARASITIC ELEMENTS OF THE  $1\ \Omega$   $R_{ds,on}$  UNIT TRANSISTOR

Parasitic element	Value	Unit	Notes
$R_{ds,on}$	1.144	$\Omega$	@ $V_{gs} = 5\ \text{V}$
$R_g$	298	$m\Omega$	
$R_{OSS}$	3.75	$\Omega$	@ $V_{gs} = 0\ \text{V}$
$C_{gs}$	28	pF	@ $V_{ds} = 5\ \text{V}$ , Freq = 250 MHz
$C_{gd}$	6	pF	
$C_{ds}$	18.48	pF	

Externally gate drives are used in implementation such as [29], [44]. One self-oscillating gate drive, commonly used in the class E converter is the class E oscillator, described in [2], [4], [28]. This procedure involves making a feedback circuit, through advanced analytic approach, but limits the duty cycle to 0.5 making it unsuitable for this design.

Recently though a new passive gate drive has been introduced in [5] and used in among others [1], [45]. In design aspects it looks like the class E oscillator, but is simpler. It is effectively an LC-filter generated by utilizing the capacitances of the MOSFET and introducing a gate-inductor. Looking at fig. 3 a schematic of the parasitics can be drawn and introducing a gate inductance,  $L_g$ , to achieve the desired filter. Fig. 8a shows the schematic for the described gate drive.

In resonant power converters, the drain voltage of the

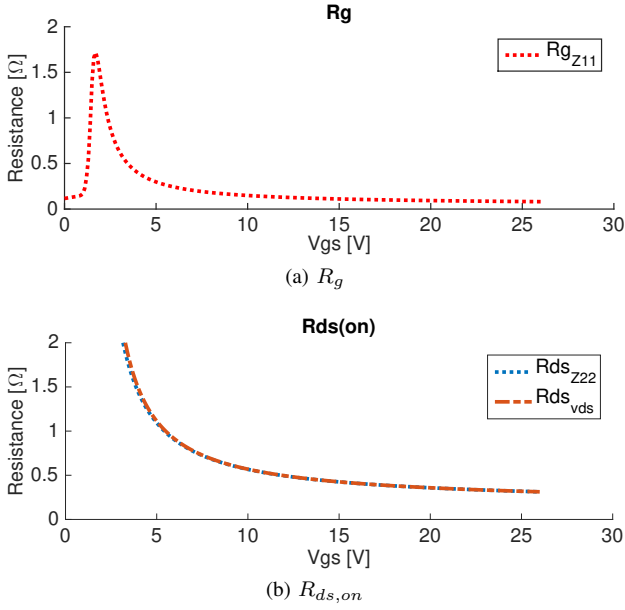


Fig. 6. Resistance of the 1-Ω Unit-transistor

transistors are close to half a sinusoidal. The added gate inductance creates a filter, with the transfer function from drain to gate shown in (23). Adjusting the inductance the poles of the filter are placed 5-10 % higher than the switching frequency, resulting in a phase shift of the drain signal as close to  $180^\circ$  as possible. This will ensure the gate signal turning on, when the voltage on the drain is zero. An added bias voltage can be tuned such that the correct duty cycle is achieved.

$$H_{Lg}(s) = \frac{(L_g s + R_g) C_{gd} s}{L_g s^2 + R_g s + \frac{1}{C_{gd} + C_{gs}}} \quad (23)$$

The introduced gate inductance will in most cases be able to give the desired phase shift at the chosen frequency. It is clear, that two zeros occur, at  $s = 0$  and  $s = -\frac{R_g}{L_g}$ . Neither of these zeros contain any imaginary parts, and the resulting frequency at which they occur is both 0.

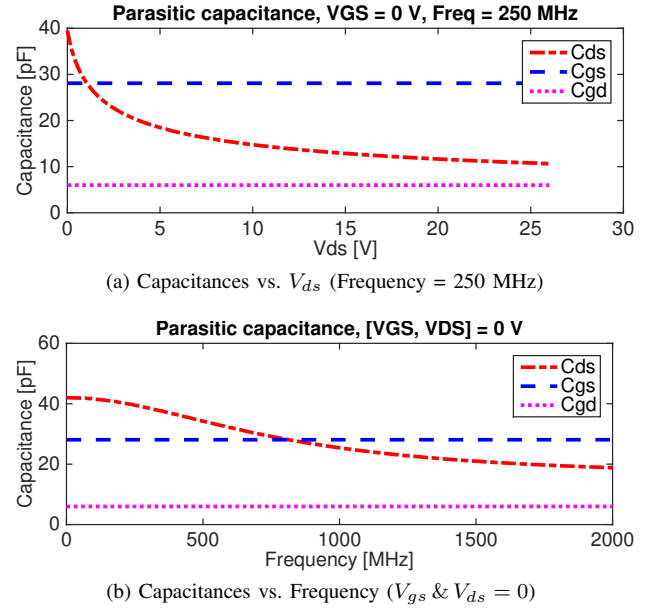


Fig. 7. Capacitances of the 1-Ω Unit-transistor

From (23) the poles of the system is found:

$$s_{pole} = \frac{-R_g \pm \sqrt{R_g^2 - \frac{4 L_g}{C_{gs} + C_{gd}}}}{2 L_g} \quad (24)$$

The poles are a complex pole pair. To determine the frequency the real and imaginary parts are found, and from the imaginary parts the frequency is found:

$$f_{pole} = \pm \frac{\Im(s_{pole})}{2\pi} = \pm \frac{\sqrt{R_g^2 - \frac{4 L_g}{C_{gs} + C_{gd}}}}{4\pi L_g} \quad (25)$$

If the attenuation achieved at the switching frequency is too high, or low, for a desired gate signal, then external capacitors can be introduced. Fig. 8b and 8c shows the schematics of the gate drives, and the transfer functions are found in (26) and (29). The zeros of these transfer functions are found using (27), (28) and (30), (31) respectively. All these equations are found at the bottom of the current page.

$$H_{Lg+Cl}(s) = \frac{(C_l L_g R_g s^2 + L_g s + R_g) C_{gd} s}{C_l L_g R_g s^3 + (1 + C_l) L_g s^2 + R_g s + \frac{1}{C_{gd} + C_{gs}}} \quad (26)$$

$$z_{1,Lg+Cl} = 0 \quad (27)$$

$$z_{2,Lg+Cl} = - \left( \frac{L_g \pm \sqrt{L_g (L_g + 4 C_l R_g^2)}}{2 C_l L_g R_g} \right) \quad (28)$$

$$H_{Lg+Ch}(s) = \frac{(C_h L_g R_g s^2 + L_g s + R_g) C_{gd} s + C_h L_g s^2}{C_h L_g R_g s^3 + (1 + C_h) L_g s^2 + R_g s + \frac{1}{C_{gd} + C_{gs}}} \quad (29)$$

$$z_{1,Lg+Ch} = 0 \quad (30)$$

$$z_{2,Lg+Ch} = - \left( \frac{(C_{gd} + C_h) L_g \pm \sqrt{L_g (L_g (C_h + C_{gd})^2 - 4 C_h C_{gd}^2 R_g^2)}}{2 C_h C_{gd} L_g R_g} \right) \quad (31)$$



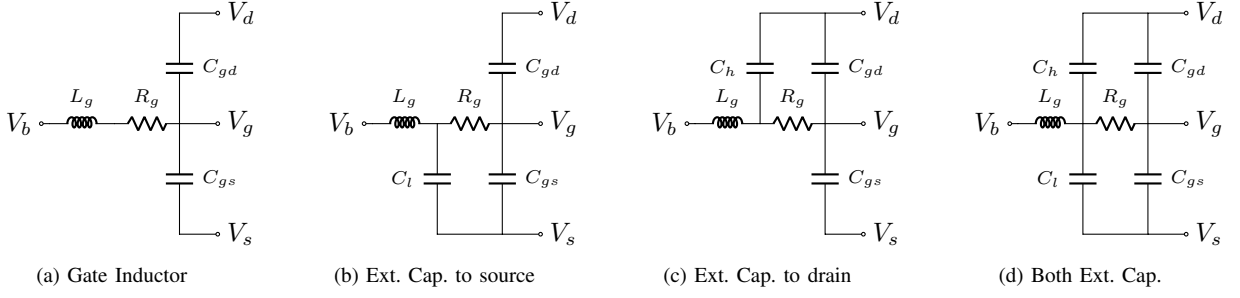


Fig. 8. Passive Gate Drives

For small values of the gate resistance these zeros are all real, so their effect will be minimal at very high frequencies. Even further any zeros effect from a higher gate resistances, can be adjusted by adding the capacitances to the gate-drain of the signal. The poles of the system are solutions to a third order polynomial, and analytically hard to interpret. From [5] a good approximation of the frequency of the pole is:

$$f_p \simeq \frac{1}{2\pi\sqrt{L_g(C_{ext} + C_{gd} + C_{gs})}} \Leftrightarrow$$

$$L_g \simeq \frac{1}{(2\pi f_p)^2 (C_{ext} + C_{gd} + C_{gs})} \quad (32)$$

This is the resonant frequency neglecting the gate resistance. As with the previous gate drives, the resonance frequency is desired to be kept a little higher than the switching frequency of the converter.

The final simple gate drive that can be designed is adding both the external capacitance to source and to drain, shown in fig. 8d. Using external capacitance can be an advantage because it gives the option for more linear capacitances (i.e Metal-Insulator-Metal (MIM) capacitors on chip) than the intrinsic capacitance of the MOSFET, and thus better control of the gate signal. The transfer function of the gate drive with both capacitors is seen in (33).

The zeros are found similarly to the other gate drives, see (34) and (35). The gate resistance has an influence on the zeros, if it is large enough, however this influence can be tuned, by adjusting the external capacitances.

As with the previous gate drives, analytically investigating the poles is unfruitful but using (32) is still a good approximation of the poles frequency. The gate resistance has a very real effect on the achievable phase shift of the gate drive, and in a transistor design should be kept as low as possible to avoid the effects of the zeros.

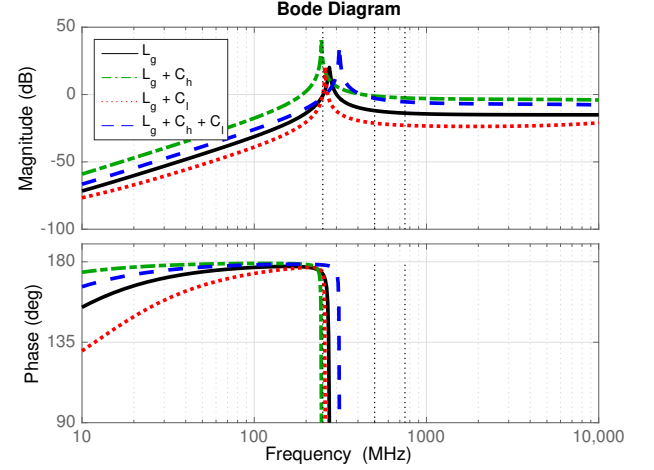


Fig. 9. Gate Drives designed

In table IV the four different gate drives designed are listed. They are all designed for a 10x1-Ω-unit transistor. The design of the gate drives was focused on achieving similar performance, while reducing component sizes. The bode plots of the resulting transfer functions are shown in fig. 9. Adding the external capacitors result in a smaller inductor, a component desired to keep as small as possible, when designing the integrated circuit.

### E. Inductors

There is several methods to choose from, when designing an inductor on a chip. From the more simple ones using a planar spiral [46]–[49], to toroids [50], [51], and also using magnetic films to reduce the required size of the inductors [8],

$$H_{Lg+Ch+Cl}(s) = \frac{(C_h + C_l) L_g R_g C_{gd} s^3 + (C_{gd} + C_h) L_g s^2 + C_{gd} R_g s}{(C_h + C_l) L_g R_g s^3 + (C_h + C_l) L_g s^2 + R_g s + \frac{1}{C_{gs} + C_{gd}}} \quad (33)$$

$$z_{1,Lg+Ch+Cl} = 0 \quad (34)$$

$$z_{2,Lg+Ch+Cl} = - \left( \frac{(C_{gd} + C_h) L_g \pm \sqrt{L_g \left( L_g (C_h + C_{gd})^2 - 4 (C_h + C_l) C_{gd}^2 R_g^2 \right)}}{2 (C_h + C_l) C_{gd} L_g R_g} \right) \quad (35)$$

TABLE IV  
RESULTING COMPONENT SIZES, ATTENUATION AND PHASE SHIFT OF THE GATE DRIVES

	Gate Inductor	Ext. Cap. to source	Ext. Cap. to drain	Both Ext. Cap ( $C_l$ & $C_h$ )
$L_g$	1 nH	400 pF	500 pF	250 pF
$C_l$	-	610 pF	-	300 pF
$C_h$	-	-	200 pF	400 pF
$ H $ at 250 MHz	-0.77 dB	-0.49 dB	-0.35 dB	-2.03 dB
$\angle H$ at 250 MHz	173.3 °	173 °	177.5 °	178.23 °

[18], [19]. The main concern is the achievable Q values - the relation between its inductive value, frequency and resistive value. In an integrated circuit the close proximity to the highly conducting silicon layer results in very high losses from eddy currents induced.

Increase of the Q values is the subject of substantial research. In [49] Q values as high as 50 at 7GHz was achieved. These where, however, constructed in a very fragile structure, and not suitable for most application. Others have tried different shielding methods, to remove the capacitive coupling to the substrate [46]. This limits the self-resonance significantly [52]. The toroidal designs presented in [50], [51] although producing promising results on the Q values of the inductors, as high as 50, the frequencies of these technologies are also currently limited around 10 MHz [8].

The research in this field is in fast development, and is one of the key components to achieving the monolithically integrated power supply. The inductors lack in both modeling for simulations, and in the achievable Q-value. Gardner et. al. [18] made an overview of on-chip inductors, and the only inductors usable in frequencies above 100 MHz are planar spiral structured air inductors. These inductors have not shown Q values above 10. Very recently Ferric Inc. introduced post-processed inductors on chip, capable of handling frequencies at 50-150 MHz, with magnetic thin film [53]. Sturcken et.al. demonstrated in a 1.8V to 1V integrated voltage regulator, with efficiencies  $\sim 70\%$ . [54] These inductors was, however, not available for this work. Lastly, it is worth mentioning that another solution could be bond wires. With inductance values around 1nH/mm and Q values approaching 50 at 1 GHz they

are very interesting. Automated setups can keep variations of inductance to within 1% [55]. Nonetheless, in this work, the fully monolithic integration was of highest priority and bond wires were therefore ruled out.

In this paper the lump-model of a spiral inductor on chip is used, obtained from [55], shown in fig. 10. It consist of an inductance  $L$ , a series resistance  $R_s$ , together with a resistance associated with the eddy-current losses induced in the substrate,  $R_{eddy}$ . It has parasitic capacitances both to the substrate,  $C_{ox}$  and to the cross under path,  $C_p$ , which is needed to connect the innermost winding to the outside. Finally there are parasitics associated with the substrate, both its resistivity,  $R_1$  and capacitance,  $C_1$ .

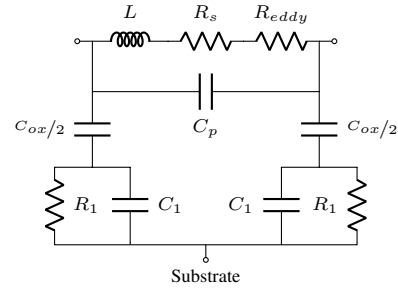


Fig. 10. Inductormodel based on [55]

Three octagonal inductors used in the simulations are here presented. The inductors are all designed from the process parameters for the current process, using the top metal layer, farthest from the silicon, and largest thickness. The results is shown in table V. The Q value of 14 is higher than described in the literature. This is due to the crudeness of the model, and the results would have to be verified before an actual implementation.

Fig. 11 shows the Q value over frequency of the designed inductors. The two larger inductors have an optimum around 200 MHz, and decreases, until their self resonance frequency of approximately 2 GHz at which Q is zero. The 750pH inductor can be seen to have a maximum much higher, at a frequency close to 3 GHz. For all of the above described inductors their self resonance frequency is well above the desired switching frequency of the circuit.

TABLE V  
DESIGN OF THE INITIAL INDUCTORS

Inductor	L [H]	$R_s$ [m $\Omega$ ]	$R_{eddy}$ [ $\mu\Omega$ ]	$C_p$ [fF]	$C_{ox}$ [fF]	$R_1$ [ $\Omega$ ]	$C_1$ [fF]	Q @ 250 MHz
$L_{in}$	750p	193.5	12.4	116.6	303.8	469.5	21.3	6.1
$L_{r,i}$	3.5n	294.8	846.7	859.9	2730	52.14	191.8	15.6
$L_{r,r}$	4.5n	338.7	2010	1070	3920	36.34	275.8	14.8

TABLE VI  
DESIGN OF THE FINAL INDUCTORS

Inductor	L [H]	$R_s$ [m $\Omega$ ]	$R_{eddy}$ [ $\mu\Omega$ ]	$C_p$ [fF]	$C_{ox}$ [fF]	$R_1$ [ $\Omega$ ]	$C_1$ [fF]	Q @ 250 MHz	Tr. W. [ $\mu m$ ]	Est. Area [ $mm^2$ ]
$L_{in}$	550p	200.52	4.26	59.51	159.03	896.83	11.15	4.31	25	0.033
$L_{r,i}$	1.8n	430.19	85.39	107.12	494.75	288.27	34.69	6.52	30	0.15
$L_{r,r}$	4n	581.14	258.09	204.11	912.30	156.33	63.96	10.33	35	0.18
$L_{gate}$	300p	121.86	2.16	64.27	140.15	1020	9.83	3.87	30	0.031

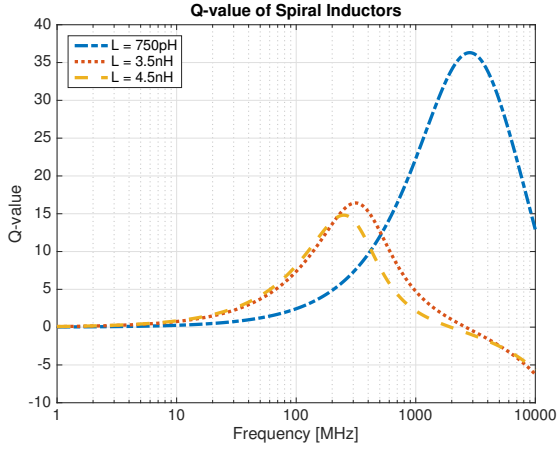


Fig. 11. Q value of the designed Inductors over Frequency

### III. RESULTS

Referring back to the design flowchart in fig. 1, a switching frequency has to be selected. To achieve the smallest possible converter, the highest possible switching frequency is desired. From (9) the shunt capacitance in the rectifier is inverse proportional to the frequency. If a switching frequency of 500 MHz is chosen, the resulting capacitance of the transistor will be so small that the resulting drain-source resistance gives a conduction loss above 20 % of the total power.

To address this issue, the switching frequency is decreased. Several steps were taken in this design procedure, and three different converters were designed. All designs were made with MIM-capacitors, and ideal inductors.

- A 250 MHz design with 22 parallel coupled 1- $\Omega$ -unit transistor in the inverter
- A 150 MHz design with 22 parallel coupled 1- $\Omega$ -unit transistor in the inverter
- A 250 MHz design with 10 parallel coupled 1- $\Omega$ -unit transistor in the inverter

The first design had issues with currents induced through the gate-drain capacitor to the drain channel because of the large capacitive value and a high  $dv/dt$  of the gate-signal. As a result two other designs were made, lowering the frequency, and with a smaller device (i.e. lowering the gate capacitance). Although the 150 MHz design showed improvement in terms of efficiency, their respective inductors was twice as large in physical size. The power density became much lower than desired. In the end, the 250 MHz design with the 10x1- $\Omega$ -unit

transistor was chosen for further implementation, with the self oscillating gate drive because of its smaller size. The results of the converters designed are shown in table VII.

#### A. 250 MHz Converter with Self Oscillating Gate Drive

The 250 MHz design is implemented with the self-oscillating gate drive with both external capacitors to ground and drain respectively. Fig. 12 and 13 presents the simulation results. The switching frequency achieved is 272 MHz.

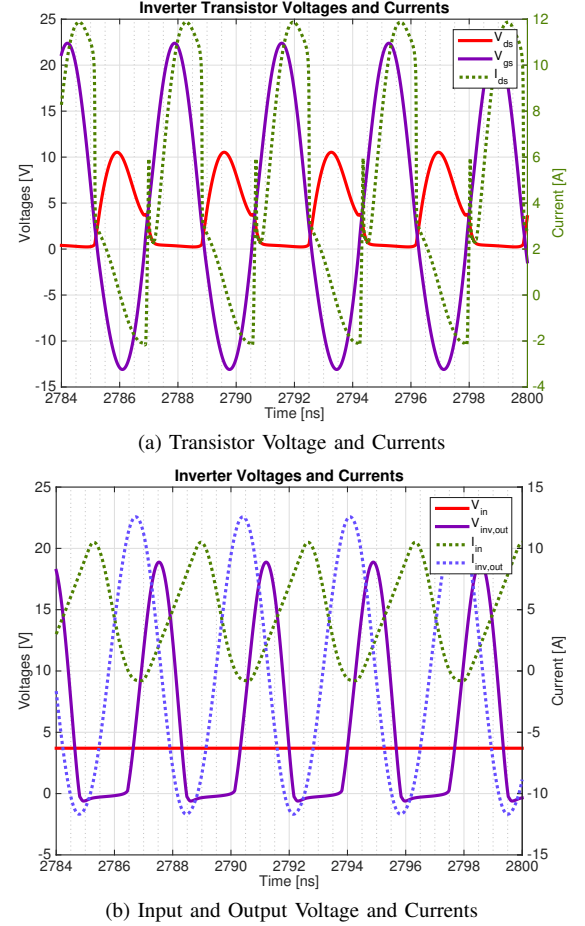


Fig. 12. Inverter waveforms of the 250 MHz Converter with Self Oscillating Gate Drive

The circuit has been tuned for optimum performance, and the self resonance of the circuit became a little higher. Due to the nature of the self oscillating gate drive, no adjustment is needed in the gate drive. The gate signal has a peak-to-peak

TABLE VII  
SUMMARY OF DESIGNED CONVERTERS

	Inverter			Rectifier			Power	
	$V_{DS,i,pk}$ [V]	$I_{sw,rms}$ [A]	$I_{out,pp}$ [A]	$V_{DS,r,pk}$ [V]	$I_{sw,rms}$ [A]	$I_{out,ripple}$ [mA]	$P_{avg,in}$ [W]	$\eta$ [%]
250 MHz (22x1 $\Omega$ -unit transistor)	15.45	8.8	8.52	27.44	2.62	1.22	22.14	43.21
150 MHz (22x1 $\Omega$ -unit transistor)	14.47	5.32	6.73	27	2.54	3.1	14.71	64.84
250 MHz (10x1 $\Omega$ -unit transistor)	13.46	6.25	10.56	20.89	2.9	3.62	17.24	52.1

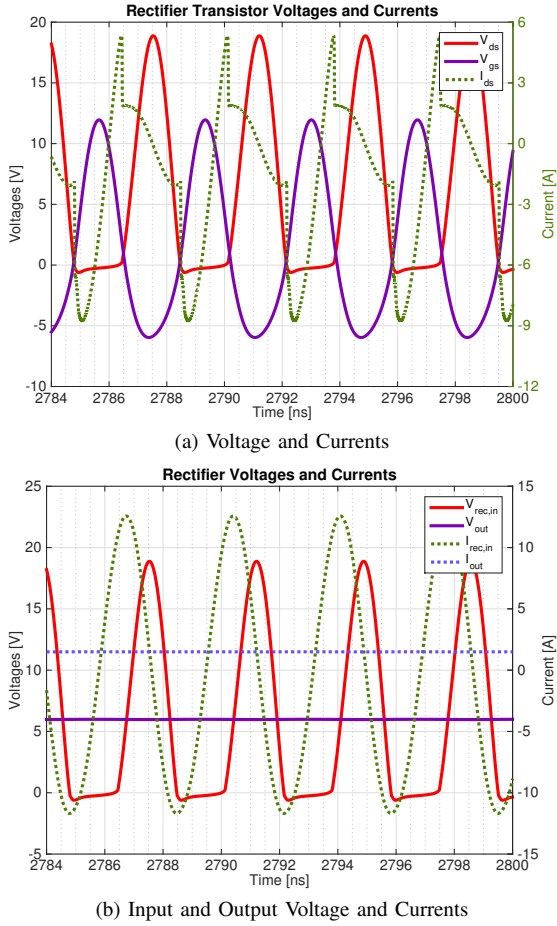


Fig. 13. Rectifier waveforms of the 250 MHz Converter with Self Oscillating Gate Drive

amplitude of 33V, and from (13) this will result in a high loss in charging and discharging of the gate capacitances.

The duty cycle achieved is 46 % and 43 % in the inverter and rectifier respectively. The results are close to the expected in the rectifier, but the duty cycle achieved in the inverter is smaller. Tuning the bias to increase the duty cycle unfortunately was not possible, without compromising the breakdown voltage on the gate. The drain current of the transistor is seen to spike just at turn off, and not achieving ZCS. However, ZVS is achieved, naturally by the self-oscillating gate drive. The efficiency of the converter is 55.5 %, which is comparable to other PwrSoC designs [8]. To understand the power losses in the circuit, the losses in the transistors were calculated according to section II-B. The results are presented in table VIII and fig. 14. The RMS currents were extracted from the resulting simulations.

 TABLE VIII  
POWER LOSSES IN THE TRANSISTORS

	Inverter [W]	Rectifier [W]
$P_{cond}$	2.15	0.76
$P_{off,cond}$	0.42	0.35
$P_{gate}$	2.52	0.66
$P_{tot}$	5.09	1.77

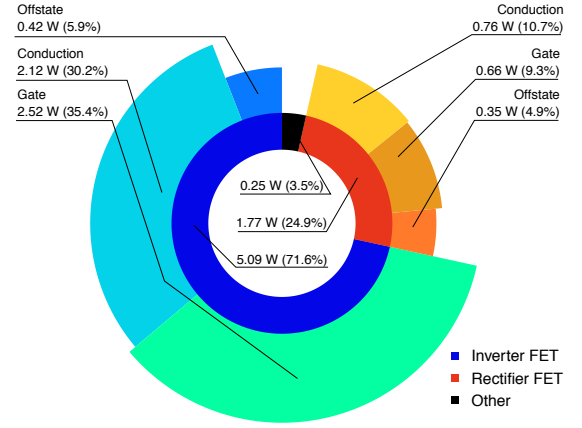


Fig. 14. Power Loss Breakdown in the 250 MHz Converter with Self Oscillating Gate Drive

The total loss in the transistors is close to 6.85 W. The converter has been tuned for an output power of 9 W, and had a total average input power of 16.11 W. The remaining losses of 0.25 W can be contributed to the ESR of the MIM capacitors. The results of the converter with the self oscillating gate drive are shown in table IX.

With a loss of approximately 7W, the design of the thermal handling also becomes important. If 100 K temperature rise is allowed, from ambient, then the thermal resistivity from silicon to the ambient surroundings cannot exceed 14 K/W. The estimated overall size of the final converter, assuming MIM-capacitors of 3 fF/ $\mu\text{m}^2$ , and no overlaying of capacitors or inductors, is 28.6 mm<sup>2</sup>. This gives a power density of 0.314 W/mm<sup>2</sup>.

 TABLE IX  
SUMMARY OF 250 MHz CONVERTER WITH 10X1Ω-UNIT TRANSISTOR IN THE INVERTER AND SELF OSCILLATING GATE DRIVE

Inverter	
$V_{ds,pk}$	10.53
$I_{sw,rms}$	7
$I_{out,pp}$	24.25
Rectifier	
$V_{ds,pk}$	18.88
$I_{sw,rms}$	4.13
$I_{out,ripple}$	5.1
Power	
$P_{avg,in}$ [W]	16.11
$\eta$ [%]	55.54

### B. Implementing Inductor Models

The results shown so far have been simulations with ideal inductances. A simulation with the presented model for inductors was carried out. However the inductors are damping the voltages of the circuit, and oscillations were not possible. Fig. 15 presents an AC analysis of the gate drive with the implemented inductors. The added parasitic resistance and capacitance of the inductors effects the gate drive, and a phase shift of over 155° is unachievable. These inductors were designed to the best performance possible, in the available IC

process, and it is very clear that these performances are just not good enough. The best available inductors integrated on chip are currently not much better than that of a standard spiral inductor, so as of right now, a different solution to the inductors has to be found. Increasing the Q factor to 10-20, showed oscillating circuits, however still with poor efficiency. One such solution could be the VHF magnetic inductors, recently introduced by Ferric Inc. [53]. These are limited at 150 MHz, so a reduction of switching frequency is an undesired side-effect. Finally, redistribution layer techniques could be implemented. Inductor values of 80 nH, with Q factors greater than 35 at 100 MHz were reported in [56].

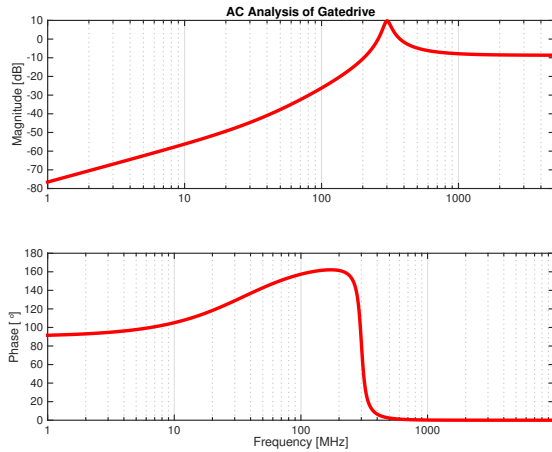


Fig. 15. AC Analysis of the Gate Drive with the Modeled Inductors

#### IV. CONCLUSION

To achieve higher power densities switching frequencies have increased. This paper presents an integrated VHF resonant power converter, switching at 250 MHz. The class E topology was deemed the most interesting for integration purposes due to lack of high side power semiconductors. However, limitations in the class E rectifier design and the process selected meant that higher switching frequencies were not desirable because of power losses. From the relations between the frequency, the capacitances in the transistors and their relation to the achievable  $R_{ds,on}$ , and the power losses in the transistors an optimum frequency for a given load and power can be found. Such an optimum could also find the best achievable inductors, either through the crude models, or using more advanced modeling. This is left for future work.

The two-port Z-parameter method was used to characterize the transistor models, utilizing the internal capacitances of the transistor in the class E converter. Furthermore the design was implemented with the self oscillating gate drive, implemented with external LC-filters. This gate drive was thoroughly mathematically analyzed, revealing the necessity to keep gate resistance at a minimum, to achieve the best performance. The four designed converters were designed for a 9W output power in a 4- $\Omega$  load, and efficiencies in the range from 43-64 % were reached. With the self oscillating gate drive the simulated efficiency with ideal inductors was 55 %. The power density based on simulations with ideal

inductor models was 0.314 W/mm<sup>2</sup>. However implementing models of integrated spiral inductors showed that the added parasitics lowers the performance of the gate drive, eliminating the possibility for ZVS. Other methods of implementing the inductors are necessary, for a working integrated resonant power converter with this type of gate drive.

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